What is claimed is:

1. A data transfer control apparatus comprising:

a bus master;

a bus interface connected to said bus master via a master bus;

a plurality of bus slaves connected to said bus interface via a slave bus;

a transfer bus which connects a first bus slave and a plurality of second bus slaves in said plurality of bus slaves;

a selection section which outputs a select signal for selecting one of said plurality of second bus slaves;

a transfer instruction section which outputs a transfer instruction signal for instructing whether or not to execute data transfer via said transfer bus; and

a transfer control section which controls data transfer via said transfer bus between said second bus slave selected by said select signal and said first bus slave in response to a control signal output to said slave bus when an instruction is given by said transfer instruction signal.

2. The data transfer control apparatus according to claim 1, wherein said first bus slave is constituted by a memory, and said transfer instruction section determines whether or not to execute data transfer via said transfer bus in accordance with address space of said memory specified by an address signal output to said slave bus and

sends said transfer control section said transfer instruction signal depending on what determination is done.

3. The data transfer control apparatus according to claim 1, wherein said transfer instruction section is included in said bus master which outputs said transfer instruction signal for instructing whether or not to execute data transfer via said transfer bus.

4. The data transfer control apparatus according to claim 3, wherein said selection section is included in said bus master which outputs said select signal for selecting one of said plurality of second bus slaves.

5. The data transfer control apparatus according to claim 4, wherein said first bus slave is constituted by an external device control section for controlling an external device connected outside, and said transfer control section controls data transfer via said transfer bus between said second bus slave selected by said select signal and said external device via said external device control section in response to a control signal output to said slave bus and information which is output from said external device control section and defines said external device, when said transfer instruction signal instructs execution of data transfer via said transfer bus.

6. The data transfer control apparatus according to claim 1, wherein each of said plurality of second bus slaves is constituted by a plurality of modules respectively allocated to different address spaces, and said selection section outputs a select signal for selecting one of said plurality of modules in accordance with that address space specified by an address signal output to said slave bus.

7. The data transfer control apparatus according to claim 6, wherein said bus master sends said selection section said address signal to specify one of said plurality of modules and said selection section outputs said select signal for selecting one of said plurality of modules in response to said address signal from said bus master.

8. The data transfer control apparatus according to claim 5, further comprising a second bus master and a second bus interface connected to said second bus master via a second master bus, wherein said second bus master executes data transfer between one of said plurality of second bus slaves via said second bus interface concurrently with data transfer which is carried out via said transfer bus between said second bus slave selected by said select signal and said external device via said external device control section under control of said transfer control section.

9. The data transfer control apparatus according to

claim 8, wherein said transfer control section inhibits access to said bus interface connected to said first bus slave by sending a busy signal indicative of data transfer in progress to that bus interface when receiving said transfer instruction signal from said bus master, and said bus master executes data transfer to one of said plurality of second bus slaves via said second bus interface without waiting for completion of data transfer being executed to said external device via said transfer bus through said external device control section, after receiving a transfer instruction acceptance signal representative of acceptance of said transfer instruction signal from said transfer control section in response to said transfer instruction signal.

10. The data transfer control apparatus according to claim 8, wherein said bus master supplies said bus interface a slave bus acquisition request signal for acquiring a bus access, and said bus interface which has received said slave bus acquisition request signal executes data transfer between said first bus slave and one of said plurality of second bus slaves without accepting an access request from said bus master or said second bus master.